AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A data processing device comprising:

a plurality of connection terminals for being individually supplied with signals, including processing data, a clock signal, and a reset signal, and drive electric power;

at least one radio antenna for receiving said signals and said drive electric ~~poser~~ power as one radio wave;

a data processing circuit switchable between a terminal mode, in which only the signals supplied to said connection terminals are effective, and an RF mode, in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with ~~said~~ the drive electric power and said signals; and

a mode selecting circuit for setting said data processing circuit to ~~said~~ the RF mode by default in response to ~~said~~ the drive electric power starting to be supplied, and for switching to said terminal mode in response to the clock signal and the reset signal ~~which are~~ being applied to corresponding ones of said connection terminals.

2. (Currently amended) A data processing device according to claim 1, wherein said mode selecting circuit ~~has~~ comprises mode maintaining means for maintaining ~~said~~ the terminal mode until the supply of ~~said~~ drive electric power is stopped.

3. (Currently amended) A data processing device according to claim 1, wherein said mode selecting circuit comprises:

clock counting means for counting clock pulses of the clock signal supplied in response to ~~said~~ the drive electric power starting to be supplied; and

input deciding means for outputting a switching signal to switch said data processing circuit to said terminal mode when said clock counting means has counted a predetermined number of clock pulses.

4. (Currently amended) A data processing device according to claim 3, wherein said input deciding means ~~has~~ comprises data output means for outputting ~~said~~ the reset signal as ~~said~~ the switching signal when said clock counting means has counted a predetermined number of clock pulses.

5. (Currently amended) A data processing device according to claim 3, wherein said mode selecting circuit ~~has~~ comprises mode maintaining means for applying ~~said~~ the switching signal output by said input deciding means as a dummy clock signal to said clock counting means through a feedback loop.

6. (New) A data processing device according to claim 5, wherein said mode selecting circuit includes a mode maintaining circuit for outputting the switching signal as the dummy clock signal.

7. (New) A data processing device according to claim 1, further comprising a power extracting circuit for extracting the drive electric power from the radio wave.

8. (New) A data processing device according to claim 1, wherein said mode selecting circuit comprises:

a clock counter responsive to the initial application of the drive electric power for counting clock pulses of the clock signal supplied to the respective one of said connection terminals; and

said input deciding circuit is responsive to said clock counter counting a predetermined number of clock pulses, for providing the reset signal as the switching signal.

9. (New) A data processing device according to claim 8, wherein said mode selecting circuit provides the switching signal as a dummy clock signal to said clock counter.

10. (New) A data processing device according to claim 3, further comprising a power extracting circuit for extracting the drive electric power from the radio wave, and a power on clear circuit, responsive to the initial application of the drive electric power, for resetting said clock counter.

11. (New) A data processing device, comprising:

a plurality of connection terminals adapted to be supplied respectively with processing data, a clock signal, a reset signal, and drive electric power;

at least one radio antenna for receiving the processing data, the reset signal, and the drive electric power in a radio wave;

a data processing circuit switchable between a terminal mode, in which only the signals supplied to said connection terminals are effective, and an RF mode, in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with the drive electric power and the signals; and

a mode selecting circuit responsive to initial application of the drive electric power to said data processing device for setting said data processing circuit to one of the terminal mode and the RF mode, and further responsive to the state of the clock and reset signals for applying a switching signal to said processing circuit to switch said data processing circuit to the other of the terminal mode and the reset mode.

12. (New) A data processing device, comprising:

a plurality of connection terminals adapted to be supplied respectively with processing data, a clock signal, a reset signal, and drive electric power;

at least one radio antenna for receiving processing data, the reset signal, and drive electric power in a radio wave;

a data processing circuit switchable between a terminal mode, in which only the signals supplied to said connection terminals are effective, and an RF mode, in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with the drive electric power, the processing data, and the signals; and

a mode selecting circuit responsive to initial application of the drive electric power to said data processing device for setting said data processing circuit to the RF mode, and further responsive to receipt of the clock and reset signals for applying a switching signal to said data processing circuit to switch said data processing circuit to the terminal mode.

13. (New) A data processing device according to claim 12, wherein said mode selecting circuit maintains said data processing circuit in the terminal mode until the supply of drive electric power is stopped.

14. (New) A data processing device according to claim 12, wherein said mode selecting circuit comprises:

a clock counter responsive to the initial application of the drive electric power for counting clock pulses of the clock signal supplied to the respective one of said connection terminals; and

an input deciding circuit responsive to said clock counter counting a first predetermined number of clock pulses, for outputting a switching signal to switch said data processing circuit to the terminal mode.

15. (New) A data processing device according to claim 14, wherein said input deciding circuit is responsive to said clock counter counting a second predetermined number of clock pulses, for providing the reset signal as the switching signal.

16. (New) A data processing device according to claim 14, wherein said mode selecting circuit provides the switching signal as a dummy clock signal to said clock counter.

17. (New) A data processing device according to claim 16, wherein said mode selecting

circuit includes a mode maintaining circuit for outputting the switching signal as the dummy clock signal.

18. (New) A data processing device according to claim 14, further comprising a power extracting circuit for extracting the drive electric power from the radio wave, and a power on clear circuit, responsive to the initial application of the drive electric power, for resetting said clock counter.

19. (New) A data processing device according to claim 12, further comprising a power extracting circuit for extracting the drive electric power from the radio wave.

20. (New)A data processing device according to claim 12, wherein said mode selecting circuit comprises:

a clock counter responsive to the initial application of the drive electric power for counting clock pulses of the clock signal supplied to the respective one of said connection terminals; and

said input deciding circuit is responsive to said clock counter counting a second predetermined number of clock pulses, for providing the reset signal as the switching signal.

21. (New) A data processing device according to claim 12, wherein said mode selecting circuit provides the switching signal as a dummy clock signal to said clock counter.